REMARKS

Claims 25-32, 34-37, and 39-53 are pending in this application. Claims 1-24, 33, and 38 have been canceled without prejudice and claim 26 is withdrawn from consideration. By this Amendment, claims 25, 27, 29, 31, 34, 35, 39, 40, 45, and 47-53 have been amended. The amendments made to the claims do not alter the scope of these claims, nor have these amendments been made to define over the prior art. Rather, the amendments to the claims have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

The claims were previously rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6, 500,715 ("*Matsuzaki*") and claims 43 and 44 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Matsuzaki* in view of *Sani*. Applicants respectfully traverse these rejections.

Among the limitations of independent claim 29 not present in Matsuzaki are "an edge-triggered flip-flop comprising a storage flip-flop subcircuit ... [and] a pulse generator circuit that generates a flip-flip input signal from an input signal and from a clock signal and is coupled to the first power switch transistor and to the switching transistors."

The above-recited features are similar to features appearing in independent claims 51, 52 and 53. It should be noted that these features are disclosed in the specification at least in paragraphs 93 and 94.

Figure 14 of *Matsuzaki* does not show *an edge-triggered flip-flop*, which comprises a storage flip-flop subcircuit having a plurality of storage transistors, a first power switch transistor, a plurality of switching transistors for coupling a flip-flop input

signal into the storage flip-flop subcircuit, and a pulse generator circuit that generates a flip-flop input signal, as recited in claim 29 (similarly amended claims 51 to 53). Fig.14 shows an integrated circuit, including a three-stage CMOS inverter (TP1, TN1, TP2, TN2, TP3, TN3) and a level holder circuit (LH1). However, neither the level holder circuit (LH1) alone nor the integrated circuit of Fig.14 as a whole form an *edge-triggered flip-flop* having the above-cited features as recited in claim 29 of the present patent application. Furthermore, even *Matsuzaki* taken as a whole does not disclose an edge-triggered flip-flop as described above. The subject matter of amended claim 29 is thus novel over *Matsuzaki.* The same holds true for amended claims 51 to 53 which recite similar limitations.

In accordance with claims 29, 51, 52 and 53, circuit designs are provided for an edge-triggered flip-flop, by which circuit designs a high signal speed as well as a permanent storage capability in a standby mode are made possible in the edge-triggered flip-flop with a very low outlay. This is clearly achieved by combining the advantages of transistors having a high threshold voltage (low leakage current) with the advantages of transistors having a low threshold voltage (low signal delay and attenuation) and realizing subcircuits of the edge-triggered flip-flop, i.e., a storage flip-flop subcircuit, a pulse generator subcircuit, a power-switch subcircuit and a coupling-in subcircuit, by using and coupling the appropriate transistors in the way described in claims 29, 51, 52 and 53. Thus, an edge-triggered flip-flop is realized that has a high signal speed during normal operation as well as a reliable retention of the storage content during a standby mode.

Matsuzaki neither discloses nor suggests an edge-triggered flip-flop having the features as recited in any one of amended claims 29, 51, 52 and 53 of the present patent application.

Claims 39 to 42 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over *Matsuzaki* in view of *Sani.*

Sani discloses an integrated circuit including a Multi-Theshold CMOS (MTCMOS) latch combining low voltage threshold CMOS circuits with high voltage threshold CMOS circuits. However, also *Sani* neither discloses nor suggests an edge-triggered flip-flop in accordance with any one of claims 29, 51, 52 and 53. *Sani* thus fails to cure the deficiencies of *Matsuzaki.*

As none of the above-cited documents, taken alone or in combination, discloses or suggests the subject matter as claimed by amended claim 29, the subject matter of amended claim 29 is believed to be non-obvious over the cited prior art documents of *Matsuzaki* and *Sani.* The same holds true for amended claims 51 to 53, which recite similar limitations. Claims 29, 51, 52, and 53 are non-obvious over the applied prior art. Because the other claims in the present application are ultimately dependent on one of these claims, they are believed to be non-obvious for at least the same reasons.

Applicants note that claim 25 has been amended to correspond to claim 29. The references in claims 27, 34, and 35 have been corrected. In claim 31, a typographical error was corrected. In claim 39, it has been clarified that the test circuit is coupled to the storage flip flop subcircuit and tests the functionality of the storage flop subcircuit. In claim 40 it has been clarified that a test input signal is programmed into the storage flip-flop subcircuit and that a test output signal is read out from the storage flip-flop subcircuit. Claims 45, 47, and 48 have been clarified in that the protection transistors are located between the storage flip-flop subcircuit and the switching transistors and that the protection transistor selectively couple or decouple the storage

flip-flop subcircuit from the switching transistors. Finally, claims 49 and 50 have been amended in accordance with the amendments of claims 45, 47, and 48.

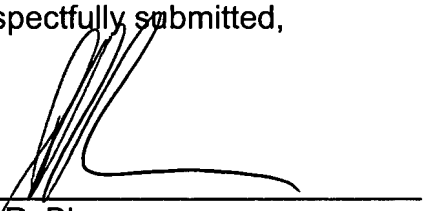
Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: May 11, 2007

Respectfully submitted,



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